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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. **MCT.0102US**

In Re Application Of: **Paul Petersen**

Serial No.	Filing Date	Examiner	Group Art Unit
09/419,523	**October 18, 1999**	**Christian Chace**	**2187**

Invention: **Determining Memory Upgrade Options**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **January 28, 2003**

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☒ A check in the amount of the fee is enclosed.

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A duplicate copy of this sheet is enclosed.

Signature

Dated: **March 31, 2003**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Paul Petersen	§	Group Art Unit:	2187
Serial No.:	09/419,523	§	Examiner:	Christian Chace
Filed:	October 18, 1999	§		
For:	Determining Memory Upgrade Options	§	Atty. Dkt. No.:	MCT.0102US MUEI-0521.00/US

Board of Patent Appeals & Interferences
Commissioner for Patents
Washington, D.C. 20231

APPEAL BRIEF

Dear Sir:

Applicant hereby appeals from the Final Rejection dated October 28, 2002, finally rejecting claims 1-40.

I. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

Date of Deposit: March 31, 2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated above and is addressed to the Board of Patent Appeals & Interferences, Commissioner for Patents, Washington, DC 20231.
Debra Cutrona

III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-20. Claims 21-40 were added during prosecution of the application. Claims 1-40 have been finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

There are no unentered amendments.

V. SUMMARY OF THE INVENTION

Techniques (including methods and devices) are described to determine a memory configuration of a computer system and provide memory upgrade options to a user. The following embodiments of this invention are illustrative only and are not to be considered limiting in any respect. Specification, p. 2.

Referring to FIG. 1, an illustrative computer system 100 in accordance with the invention includes a memory configuration routine 112 to determine characteristics of system memory 110 and provide this information to a user in anticipation of a memory upgrade. The routine 112 determines the memory address characteristics of the system 100 (e.g., maximum address space of a processor/operating system and/or number of memory sockets available for connecting memory). The routine 112 also identifies a current memory configuration including the operational characteristics of installed memory. Using this combination of information, the routine 112 calculates a residual memory capacity and provides memory upgrade options to a user. Illustrative operational characteristics include, but are not limited to, the type of memory,

the operating speed of the memory, the size or capacity of the memory, and the organization (i.e., bank layout) of the memory. Specification, pp. 2-3.

As shown, the system 100 may also include a processor 102 coupled to a host bridge circuit 106 through a processor bus 104. The host bridge circuit 106 (such as the 82443BX Host-to-PCI bridge device from Intel Corporation) may facilitate communication between the processor 102 and various other system devices, including system memory 110. A memory controller 108 may be included in the host bridge circuit 106 to control access to the system memory 110. When the processor 102 or another device of the system 100 requires access to the system memory 110, the memory controller 108 must be activated. Specification, p. 3.

The host bridge circuit 106 may be coupled to a primary bus 118 which operates in conformance with, for example, the Peripheral Component Interconnect (PCI) standard. An expansion bridge circuit 116, (such as the 82371AB PIIX4 IDE controller from Intel Corporation) allows communication between the primary bus 118 and a secondary bus 120. The secondary bus 120 may be operated in conformance with the Industry Standard Architecture (ISA), Extended Industry Standard Architecture (EISA), or the Low Pin Count (LPC) standards. Specification, p. 3.

An ancillary bus controller 117 provides a communication interface for retrieval of configuration information from system memory over an ancillary bus 119. Illustrative ancillary busses include those operated in conformance with the System Management Bus (sponsored by Intel Corporation) or the I2C bus (sponsored by Philips Semiconductors). In one embodiment of the invention, the ancillary bus controller 117 may be incorporated within the expansion bridge

circuit 116 as shown in FIG. 1. In another embodiment, the ancillary bus controller 117 may be incorporated in the host bridge circuit 106. In yet another embodiment, the ancillary bus controller 117 may be incorporated in a stand alone device coupled to primary bus 118 or secondary bus 120. Specification, p. 3.

Referring to FIG. 2, the system memory 110 may include one or more memory modules 200, each having multiple dynamic random access memory (DRAM) devices 202 and a non-volatile storage device (NVSD) 204 such as a serial presence detect (SPD) device. A memory module 200 may be a detachable device that is coupled to the system 100 through sockets which are coupled to the memory controller 110. Memory devices 202 may be arranged on the memory module 200 to provide random access memory (RAM) storage for the processor 102 and other devices of the system 100. The memory devices 202 may be any type of DRAM such as fast page mode (FPM) DRAM, extended data out (EDO) DRAM, synchronous DRAM (SDRAM), double data rate (DDR) DRAM, Synchlink DRAM (SLDRAM), or RAMBUS® DRAM (RDRAM). The non-volatile storage device 204 located on each memory module 200 may be any type of non-volatile storage, such as erasable programmable read only memory (EPROM) or electrically erasable programmable read only memory (EEPROM), that stores information about the type and operating characteristics of the memory on the module 200. Such operational characteristics include information about the memory devices' 202 speed, the total amount of memory on the memory module 200, the organization of the memory (e.g., number and size of banks) and manufacturer identification data. The ancillary bus controller 117 may query the non-volatile storage device 204 of each memory module 200 via the ancillary bus 119 to retrieve

memory configuration data to be used by the memory configuration routine 112 in determining memory upgrade options. Specification, p. 4.

Referring again to FIG. 1, the memory configuration routine 112 may be stored as an executable code segment on a program storage device 113. The device 113 may be any suitable storage media such as a magnetic hard or floppy disk drive, an optical disk drive or boot read-only memory (ROM). The memory configuration routine 112 may be provided by an original equipment manufacturer (OEM) as a utility or application that may be accessed in the same manner as conventional applications. For example, a user may launch the memory configuration routine 112 by selecting an icon or by entering text at a command prompt. Specification, pp. 4-5.

Referring to FIG. 3, the memory configuration routine 112 obtains configuration data such the type, amount and operating characteristics of memory present in system memory 110 (block 300). In one embodiment, the routine 112 may use the ancillary bus controller 117 to retrieve configuration data for currently installed memory modules 200 by querying each module's non-volatile storage device 204. In another embodiment, configuration data for each memory module 200 may stored in a non-volatile storage device 114 (see FIG. 1) when memory controller 110 is initialized during power on self test (POST) operations. Configuration data so stored may be retrieved by the routine 112. In yet another embodiment, the memory configuration routine 112 may retrieve memory configuration data form configuration registers internal to or associated with the memory controller 110 (not shown in FIG. 1). Specification, p. 5.

As shown in block 302, the memory configuration routine 112 also determines a total memory capacity for the system 100 by identifying the number of memory module sockets available and/or the number of address lines utilized by the memory controller 108. In one embodiment, basic input/output system (BIOS) routines may be used to acquire information regarding total memory capacity. Alternatively, this information may be readily available on a non-volatile storage device such as device 114 (see FIG. 1). Specification, p. 5.

In determining the total memory capacity, the memory configuration routine 112 may also account for limitations of a specific memory type already in use in the system 100. Configuration data from non-volatile storage device 204 may be utilized to determine constraints for a particular type of memory device 202. For example, if the system memory 110 comprises RAMBUS® devices, there is a limit of 32 devices per memory channel (i.e., memory devices 202). An additional limitation is that a RAMBUS® memory controller 108 may only support three memory module sockets. (A RAMBUS® technology overview may be obtained from Rambus, Inc. of California.) The precise constraints vary based on the type of memory device, but will be well known to those of ordinary skill in the art of computer system memory design. Specification, pp. 5-6.

After determining both the total memory capacity and the current memory configuration of the system 100, the memory configuration routine 112 determines memory upgrade options at block 304. For example, by contrasting the current memory configuration with the total memory capacity, the routine 112 may determine a residual memory capacity. The routine 112 may determine options to upgrade memory by adding memory modules of the same or a compatible

memory type up to the limits of the residual memory capacity. The memory configuration routine 112 may also determine options to replace existing memory modules 200 with other types of memory or with memory modules having a greater amount of memory. The options established by the routine 112 may be based on specifications of memory modules currently available through memory manufacturers. This information may be stored on the non-volatile storage device 204 or in one or more data files accessible to routine 112. Alternatively, or in addition, this information may be obtained by routine 112 via an internet connection (directly or via modem). Specification, p. 6.

Each of the possible upgrade options may be provided to a user, as shown at block 306, using any available output method such as a text listing of the options or a dialog box with upgrade information. In accordance with another embodiment, a user may be provided with an interactive interface to the memory configuration routine 112 wherein the user may be given the opportunity to select an indication of a particular memory module as an upgrade option. In response, the routine 112 may calculate new upgrade options or memory replacement options based on the user's selections. In this and similar embodiments, a user may explore many upgrade options and make an informed decision when upgrading system memory. Specification, p. 6.

VI. ISSUES

A. Can claims 1-11 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1?

B. Can claims 12-17 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 12?

C. Can claims 18-20 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 18?

D. Can claims 21-31 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 21?

E. Can claims 32-37 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 32?

F. Can claims 38-40 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 38?

VII. GROUPING OF THE CLAIMS

Claims 1-11 can be grouped together; claims 12-17 can be grouped together; claims 18-20 can be grouped together; claims 21-31 can be grouped together; claims 32-37 can be grouped together; and claims 38-40 can be grouped together. With this grouping, the claims of each group stand or fall together and do not stand or fall together with any of the claims of any of the other groups.

VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

A. Can claims 1-11 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1?

The method of independent claim 1 includes obtaining memory configuration information of a computer system. The computer system includes devices. The method includes determining a memory capacity of the computer system and determining memory upgrade options to expand the number of the memory devices based on a residual memory capacity of the computer system.

The Examiner rejects independent claim 1 under 35 U.S.C. § 103(a) as being unpatentable over the combination of U.S. Patent No. 5,280,599 (herein called "Arai") and U.S. Patent No. 5,787,464 (herein called "Yoshizawa"). Arai is generally directed to setting expanded and extended memory configurations. More specifically, Arai describes a particular type of memory addressing, called an "expanded memory configuration," that is generally described in lines 22-62 of column 1 of Arai. Arai describes another type of memory addressing, called an "extended memory configuration," that is generally described in lines 63-68 of column 1 and in lines 1-9 of column 2 of Arai. It is noted that Arai does not teach replacing, adding or removing any memory devices. Rather, Arai is generally directed toward setting a particular type of memory addressing scheme.

Yoshizawa is directed to a system in which memory devices can be added without shutting off the computer system. Therefore, Yoshizawa teaches a computer system in which memory devices can be installed while power to the computer system remains turned on. Yoshizawa does not teach criteria for determining what memory devices should be replaced, removed, added, etc.

Contrary to the limitations of claim 1, neither Arai nor Yoshizawa teaches or suggests determining memory upgrade options to expand the number of memory devices based on a residual memory capacity of a computer system. More specifically, Arai is directed toward configuring a computer to permit a user of the computer to use expanded memory space or extended memory space. However, such a disclosure does not teach or suggest the determining act of claim 1. Yoshizawa does not teach the missing claim limitations, as Yoshizawa teaches

inserting memory into expansion slots to increase a memory capacity of a computer system. However, Yoshizawa does not address determining memory upgrade options to expand the number of memory devices based on a residual memory capacity of a computer system.

To establish a *prima facie* case of obviousness, the prior art must teach all claim limitations. M.P.E.P. § 2143. The Examiner fails to meet this requirement, as neither Arai nor Yoshizawa teaches or suggests determining memory upgrade options to expand the number of memory devices in a computer system based on the residual memory capacity of the computer system. Therefore, for at least this reason, a *prima facie* case of obviousness has not been established for independent claim 1.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 1 for the additional, independent reason that the Examiner fails to provide any support for the alleged suggestion or motivation to modify either Arai or Yoshizawa to derive the missing claim limitations. In this manner, the Examiner must provide a specific citation to the prior art showing the alleged suggestion or motivation. *Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143. The Examiner has not fulfilled this requirement, as the Examiner merely concludes there would have been a suggestion or motivation for the modification with showing specific support.

Claims 2-11 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, the § 103(a) rejections of claims 1-11 are improper and should be reversed.

B. Can claims 12-17 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 12?

The program storage device of claim 12 is readable by a programmable control device. The storage device includes instructions for causing the programmable control device to obtain memory configuration of a computer system. The computer system includes memory devices. The instructions cause the programmable control device to determine a memory capacity for the computer system and determine memory upgrade options to expand the number of the memory devices based on a residual memory capacity of the computer system.

The Examiner rejects independent claim 1 under 35 U.S.C. § 103(a) in view of Arai and Yoshizawa. However, the Examiner fails to show any language in Arai or Yoshizawa that teaches instructions to cause a programmable control device to determine memory upgrade options to expand a number of memory devices based on a residual memory capacity of a computer system. Thus, for at least the reason that the Examiner fails to show where all limitations are taught in the prior art, a *prima facie* case of obviousness has not been set forth for independent claim 12.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 12 for the additional, independent reason that the Examiner fails to disclose support for the alleged suggestion or motivation to modify Arai and/or Yoshizawa to derive the missing claim limitations. In this manner, the Examiner must show the alleged suggestion or motivation to modify one of these references so that a programmable control device determines memory upgrade options to expand the number of the memory devices based on a residual memory

capacity of the computer system. Without such a showing, the Examiner has failed to establish a *prima facie* case of obviousness for claim 12 for this additional reason.

Claims 13-17 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, the § 103(a) rejections of claims 12-17 are improper and should be reversed.

C. Can claims 18-20 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 18?

The computer system of independent claim 18 includes a processor, a system memory and a configuration routine. The system memory is coupled to the processor, and the system memory has one or more memory modules and a memory configuration. The memory modules include one or more memory devices. The configuration routine includes instructions to obtain memory configuration information, determine a memory capacity of the computer system and determine memory upgrade options to expand the number of the memory modules based on a residual memory capacity.

The Examiner rejects independent claim 18 under 35 U.S.C. § 103(a) in view of Arai and Yoshizawa. However, the Examiner fails to show where the prior art teaches or suggests a configuration routine that determines memory upgrade options to expand a number of memory modules based on a residual memory capacity. Therefore, for at least this reason, the Examiner fails to establish a *prima facie* case of obviousness for independent claim 18.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 18 for the additional, independent reason that the Examiner fails to show the alleged suggestion

or motivation to modify Arai and/or Yoshizawa to derive the missing claim limitations. In this manner, the Examiner must cite specific language from a prior art reference to establish the alleged suggestion or motivation to modify Arai or Yoshizawa to teach a configuration routine that determines memory upgrade options to expand the number of the memory modules based on a residual memory capacity. As the Examiner has failed to make this showing, a *prima facie* case of obviousness has not been established for independent claim 18 for this additional, independent reason.

Claims 19 and 20 are patentable for at least the reason that these claims depend from an allowable claim.

Therefore, the § 103(a) rejections of claims 18-20 are improper and should be reversed.

D. Can claims 21-31 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 21?

The method of claim 21 includes obtaining memory configuration information of a computer system. The computer system includes memory devices. The method includes determining a memory capacity of the computer system and determining memory upgrade options to replace at least one of the memory devices based on a residual memory capacity of the computer system.

The Examiner rejects independent claim 21 under 35 U.S.C. § 103(a) in view of Arai and Yoshizawa. However, the Examiner fails to show where the prior art teaches or suggests determining memory upgrade options to replace at least one of multiple memory devices of a computer system based on a residual memory capacity of the computer system. Therefore, for at

least this reason, the Examiner fails to establish a *prima facie* case of obviousness for independent claim 21.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 21 for the additional, independent reason that the Examiner fails to show specific support for the alleged suggestion or motivation to modify Arai and/or Yoshizawa so that one of these computer systems determines memory upgrade options to replace at least one of multiple memory devices based on a residual memory capacity of the computer system. Therefore, for at least this additional, independent reason, a *prima facie* case of obviousness has not been established for independent claim 21.

Claims 22-31 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, the § 103(a) rejections of claims 21-31 are improper and should be reversed.

E. Can claims 32-37 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 32?

The program storage device of independent claim 32 is readable by a programmable control device and includes instructions for causing the programmable control device to obtain memory configuration information of a computer system. The computer system includes memory devices. The instructions cause the programmable control device to determine a memory capacity for the computer system and determine memory upgrade options to replace one or more of the memory devices based on a residual memory capacity of the computer system.

The Examiner rejects independent claim 32 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Arai and Yoshizawa. However, the Examiner fails to show where the prior art teaches instructions to cause a programmable control device to determine memory upgrade options to replace one or memory devices of a computer system based on a residual memory capacity of the computer system. Without this showing, the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 32.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 32 for the additional, independent reason that the Examiner fails to show any support for the alleged suggestion or motivation to modify Arai and/or Yoshizawa to teach the missing claim limitations. Therefore, for at least this additional, independent reason, a *prima facie* case of obviousness has not been established for independent claim 32.

Claims 33-37 are patentable for at least the reason that these claims depend from an allowable claim.

F. Can claims 38-40 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 38?

The computer system of claim 38 includes a processor, a system memory and a configuration routine. The system memory has one or more memory modules and a memory configuration. These memory modules include one or more memory devices. The configuration routine includes instructions to obtain memory configuration information, determine a memory capacity of the computer system and determine memory upgrade options to replace one or more of the memory modules based on a residual memory capacity.

The Examiner rejects independent claim 38 under 35 U.S.C. § 103(a) as being unpatentable over Arai and Yoshizawa. However, the Examiner fails to establish a *prima facie* case of obviousness for at least the reason that the Examiner fails to show where the prior art teaches a configuration routine that includes instructions to determine memory upgrade options to replace one or more memory modules based on a residual memory capacity.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 38 for the additional, independent reason that the Examiner fails to show support in the prior art for the alleged suggestion or motivation to modify Arai and/or Yoshizawa so that one of these references executes a configuration routine that determines memory upgrade options to replace one or more memory modules based on a residual memory capacity. Without such a specific showing, a *prima facie* case of obviousness has not been established for independent claim 38.

Claims 39 and 40 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, the § 103(a) rejections of claims 38-40 are improper and should be reversed.

IX. CONCLUSION

The Assignee requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

Date: March 31, 2003

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APPENDIX OF CLAIMS

The claims on appeal are:

1. A method comprising:

obtaining memory configuration information of a computer system, the computer system including memory devices;

determining a memory capacity of the computer system; and

determining memory upgrade options to expand the number of the memory devices based on a residual memory capacity of the computer system.

2. The method of claim 1, wherein the act of obtaining memory configuration information comprises obtaining an indication of an installed system memory amount.

3. The method of claim 2, wherein the memory configuration information further comprises a number of memory module sockets.

4. The method of claim 2, wherein the memory configuration information further comprises an operating speed of the installed system memory.

5. The method of claim 1, wherein the act of obtaining memory configuration information comprises accessing a non-volatile storage device.

6. The method of claim 5, wherein the act of accessing a non-volatile storage device comprises accessing a serial presence detect device.

7. The method of claim 1, wherein the act of obtaining memory configuration information comprises obtaining information from one or more dynamic random access memory devices.

8. The method of claim 1, wherein the act of determining a memory capacity comprises obtaining an indication of a maximum number of memory devices for the computer system.

9. The method of claim 1, wherein the act of determining a memory capacity comprises obtaining an indication of a maximum amount of memory for the computer system.

10. The method of claim 1, wherein the act of determining a memory capacity comprises obtaining an indication of a maximum number of memory module sockets for the computer system.

11. The method of claim 1, further comprising providing memory upgrade options to a user.

12. A program storage device, readable by a programmable control device, comprising instructions for causing the programmable control device to:

obtain memory configuration information of a computer system, the computer system including memory devices;

determine a memory capacity for the computer system; and

determine memory upgrade options to expand the number of the memory devices based on a residual memory capacity of the computer system.

13. The program storage device of claim 12, wherein the instructions to obtain memory configuration information comprise instructions to obtain an indication of an installed system memory amount.

14. The program storage device of claim 13, wherein the memory configuration information further comprises a number of memory module sockets.

15. The program storage device of claim 13, wherein the instructions to obtain memory configuration information further comprise instructions to obtain an indication of a number of memory module slots available to the programmable control device.

16. The program storage device of claim 12, wherein the instructions to obtain memory configuration information comprises instructions to access a non-volatile storage device.

17. The program storage device of claim 12, wherein instructions to determine a memory capacity comprise instructions to obtain an indication of a maximum number of memory devices for the computer system.

18. A computer system comprising:

a processor;

system memory coupled to the processor, the system memory having one or more memory modules and a memory configuration, wherein the memory modules include one or more memory devices; and

a configuration routine including instructions to obtain memory configuration information, determine a memory capacity of the computer system, and determine memory upgrade options to expand the number of the memory modules based on a residual memory capacity.

19. The computer system of claim 18, wherein the instructions to obtain memory configuration information comprise instructions to obtain indications of installed memory devices.

20. The computer system of claim 18, wherein the instructions to determine a memory capacity comprise instructions to obtain an indication of a maximum amount of memory for the computer system.

21. A method comprising:

obtaining memory configuration information of a computer system, the computer system including memory devices;

determining a memory capacity of the computer system; and

determining memory upgrade options to replace at least one of the memory devices based on a residual memory capacity of the computer system.

22. The method of claim 21, wherein the act of obtaining memory configuration information comprises obtaining an indication of an installed system memory amount.

23. The method of claim 22, wherein the memory configuration information further comprises a number of memory module sockets.

24. The method of claim 22, wherein the memory configuration information further comprises an operating speed of the installed system memory.

25. The method of claim 21, wherein the act of obtaining memory configuration information comprises accessing a non-volatile storage device.

26. The method of claim 25, wherein the act of accessing a non-volatile storage device comprises accessing a serial presence detect device.

27. The method of claim 21, wherein the act of obtaining memory configuration information comprises obtaining information from one or more dynamic random access memory devices.

28. The method of claim 21, wherein the act of determining a memory capacity comprises obtaining an indication of a maximum number of memory devices for the computer system.

29. The method of claim 21, wherein the act of determining a memory capacity comprises obtaining an indication of a maximum amount of memory for the computer system.

30. The method of claim 21, wherein the act of determining a memory capacity comprises obtaining an indication of a maximum number of memory module sockets for the computer system.

31. The method of claim 21, further comprising providing memory upgrade options to a user.

32. A program storage device, readable by a programmable control device, comprising instructions for causing the programmable control device to:

obtain memory configuration information of a computer system, the computer system including memory devices;

determine a memory capacity for the computer system; and

determine memory upgrade options to replace one or more the memory devices based on a residual memory capacity of the computer system.

33. The program storage device of claim 32, wherein the instructions to obtain memory configuration information comprise instructions to obtain an indication of an installed system memory amount.

34. The program storage device of claim 33, wherein the memory configuration information further comprises a number of memory module sockets.

35. The program storage device of claim 33, wherein the instructions to obtain memory configuration information further comprise instructions to obtain an indication of a number of memory module slots available to the programmable control device.

36. The program storage device of claim 32, wherein the instructions to obtain memory configuration information comprises instructions to access a non-volatile storage device.

37. The program storage device of claim 32, wherein instructions to determine a memory capacity comprise instructions to obtain an indication of a maximum number of memory devices for the computer system.

38. A computer system comprising:

a processor;

system memory coupled to the processor, the system memory having one or more memory modules and a memory configuration, wherein the memory modules include one or more memory devices; and

a configuration routine including instructions to obtain memory configuration information, determine a memory capacity of the computer system, and determine memory upgrade options to replace one or more of the memory modules based on a residual memory capacity.

39. The computer system of claim 38, wherein the instructions to obtain memory configuration information comprise instructions to obtain indications of installed memory devices.

40. The computer system of claim 38, wherein the instructions to determine a memory capacity comprise instructions to obtain an indication of a maximum amount of memory for the computer system.